June 1969

RESEARCH AND DEVELOPMENT

OF

HIGH SPEED PROCESSOR ARRAYS

Prepared by
Philco-Ford Corporation
Microelectronics Division
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For
Massachusetts Institute of Technology
Lincoln Laboratory

THIRD INTERIM REPORT
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ABSTRACT

This report describes program developments for the third interim period of a research and development program directed toward the development of high-density, high-performance, complex digital arrays and their application in high-speed system feasibility studies.

Preliminary design for a Processor Master Array Chip containing 80 gates and 16 reference bias cells has been completed.

Functioning Read-Only Memory Arrays were successfully fabricated and delivered to MIT Lincoln Laboratory. A flexible technique for programming these ROM's at the chip level has been developed and demonstrated.

Speed-power studies aimed at obtaining optimum performance in the Processor Arrays are continuing.

Yield improvement studies are continuing. This effort includes the investigation of the applicability of the CDI process to high-speed ECL and the design of a complex Multilevel Process Test Chip for characterizing and monitoring multilevel interconnection processes and structures.

Test vehicles are being fabricated for investigating face-down bonding and aluminum beam lead technologies.

Reliability data are presented for high-speed two-level arrays.

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ILLUSTRATIONS

I - INTRODUCTION

1.1 PROGRAM OBJECTIVE

The objective of this program is the continued development of high-density, high-performance, complex digital arrays and their application in high-speed system feasibility studies.

1.2 SCOPE OF REPORT

This is a progress report for the third interim (quarterly period) of a research and development program being conducted by Philco-Ford under a subcontract with MIT Lincoln Laboratory.

1.3 AREAS OF INVESTIGATION

During the past few years, Philco-Ford has directed research and development programs toward the establishment of device, microcircuit, and large-scale array technologies which can be applied in complex, high-speed data processing systems. This has been accomplished in part on previous programs subcontracted to Philco-Ford by MIT Lincoln Laboratory under the primary sponsorship of the United States Air Force. Development of these technologies is being continued on the present program. In addition, they are being applied in the design and fabrication of a number of two- and three-level arrays as part of a program to implement LSI in feasibility studies of a high-speed Central Processor.

One of the tasks of this program is the investigation of methods for improving fabrication yields of the microcircuit and multilevel interconnection processes. Possible approaches to improving microcircuit yields include:

(1) refining conventional microcircuit processes and structures, and

(2) implementing revolutionary new processes such as the Collector Diffused Isolation (CDI) and Base Diffused Isolation (BDI) processes introduced by B. Murphy.*

Both approaches to improving the yields are being evaluated.

Program efforts also include continued investigation of multichip assembly techniques which are compatible with high speed systems. Included in this effort is a study of face-down bonding and beam lead technologies.

The layout designs of all microcircuit and array photomasks that are being used on this program is a cooperative effort between MIT Lincoln Laboratory and Philco-Ford. Lincoln Laboratory has been principally responsible for circuit design and for final design of all microcircuit and multilevel interconnect layouts. Photomasks are designed and generated through use of computer-aided mask making techniques.

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* Murphy, B. T., Neville, S. M., and Pederson, R. A., "New, Simplified, Bipolar Technology and Its Application to Systems," ISSCC Digest of Technical Papers, pp. 150-153; February 1969.

II - PROGRAM DEVELOPMENTS

2.1 SUMMARY

During this interim, preliminary design of a Processor Master Array Chip containing 80 gates was completed. This chip incorporates the basic designs for gate and reference cells which were selected during the previous interim for use in Processor Arrays.

Additional lots of SMX14 test chips were completed and are being used in yield and speed-power studies.

The first lot of 256-Bit Read Only Memory Arrays was completed. Functioning arrays were obtained from all wafers. In addition, a method for programming the ROM's at the chip level has been developed.

The Collector Diffused Isolation Process has been adopted for high speed ECL. A simple gate circuit was designed and fabricated using a form of the CDI Process. Initial performance and yield data were obtained.

The final design of the Multilevel Process Test Chip, a chip to be used for process control and for multilevel process studies, was completed. Multilevel test structures are being fabricated.

The final designs for photomasks which will adapt the Thermal Chip for face-down bonding experiments and for aluminum beam lead studies were completed during this period, and the fabrication of test structures was begun.

Forty thousand device-hours of life test reliability data have been accumulated on high speed multilevel arrays without any observed failures.

2.2 PROCESSOR MASTER ARRAY CHIP

During the previous interim, evaluations of the SMX14 test chip (containing two different gate and reference bias microcircuit designs) led to the tentative selection of basic microcircuit designs for the gate and bias reference cells to be used in the Processor Arrays. The gate operates at propagation delays on the order of 0.6 nanosecond, with a nominal power dissipation of 15 mW (fan-in and fan-out = 1). These cells were incorporated into the preliminary design of a Master Array Chip which will be used in the Processor study. The Master Array Chip is composed of 80 gate cells and 16 reference bias cells, has an area of 120 x 130 $mils^2$, and can be intraconnected through three levels of metal to form a variety of needed subfunction chips.

The Master Array Chip also offers an excellent vehicle for studying the performance of the Processor basic gate under a variety of on-chip array loading conditions. Preliminary design of a Loading Test Chip has been completed by Lincoln Laboratory.

It is expected that the final-design photomask reticles for the Master Array will be generated early during the next interim.

Fabrication will start shortly thereafter. It is also expected that photomasks for the Loading Test Chip will also be generated during the next quarter.

2.3 READ-ONLY MEMORY ARRAY (SMX15)

The first lot of 256-Bit Read Only Memory Arrays (using 256 transistors and two levels of metal) were completed during this interim. Figure 1 is a photomicrograph of an ROM Array. Functioning arrays were obtained from each wafer. The best yield obtained at die sort was 8.4%. Statistical calculations indicate that 99% transistor yields were realized on this wafer.

Programming of the high-speed SMX15 ROM can easily be accomplished at the wafer level through use of a custom designed photomask at virtually any step in the fabrication process. Quickest turn-around time using this approach is obtained by fabricating and storing wafers in nearly completed form and performing the customizing at either the insulator cut or top-level-metal etch operations. However, during the early stages of the Processor study program, it is anticipated that relatively small numbers of a large quantity of customized ROM chips will be required. In this case, the maximum flexibility and turn-around time is achieved if the ROM's are programmable at the chip level. Consequently, a mechano-chemical technique has been developed for programming the ROM top-level metal after chips have been fully

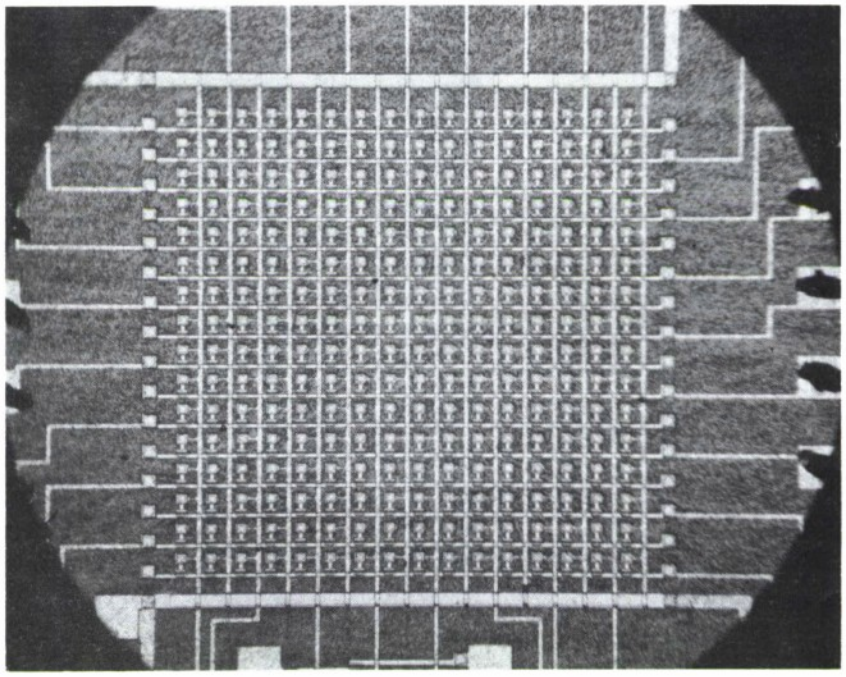

Figure 1. Photomicrograph of 256-Bit Read-Only Memory Array.

tested. This programming technique is applicable before or after the wafer is scribed, and even after chips have been bonded in a package. Figure 2 shows a high-magnification photomicrograph of a portion of an ROM chip which was programmed, after the chip was bonded in a package, by removing sections of the top-level metal at selected bit sites.

Sample programmed ROM's were delivered to Lincoln Laboratory during this interim.

Additional lots of ROM's are being processed in an effort to increase chip inventory and for purposes of studying techniques for yield improvement.

2.4 SPEED-POWER STUDIES

As indicated in subsection 2.2, a gate design which dissipates 15 mW while operating at 0.6 nanosecond propagation delays is being designed into Processor Arrays. In the meantime, speed-power studies using the SMX14 test chip are being continued to determine whether a more optimum performance compromise can be achieved. Packaged SMX15 chips on which gate dissipations were nominally 15 mW and 7.5 mW were delivered during this interim to Lincoln Laboratory for evaluation. Additional SMX15 wafers on which designed gate dissipations will be 10 mW and 5 mW are nearing completion.

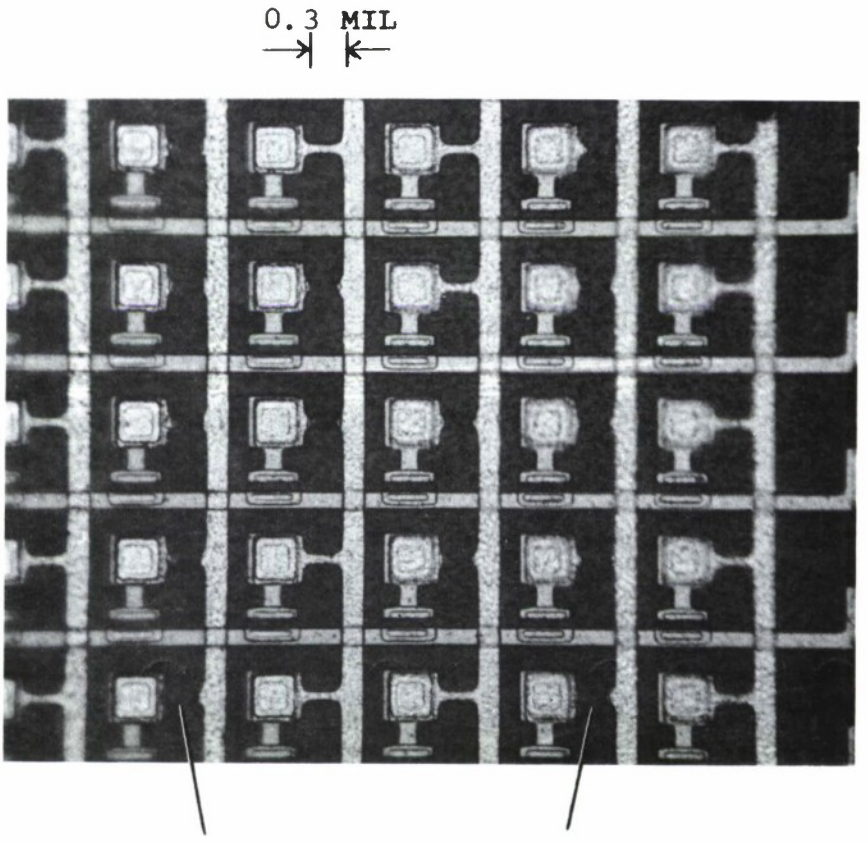

Figure 2. Photomicrograph of a programmed ROM.

2.5 YIELD IMPROVEMENT STUDIES

Studies directed toward the yield improvement in the high-performance microcircuit and multilevel interconnection processes have continued. The results of these continued studies are given in subsections 2.5.1 and 2.5.2, below.

2.5.1 Microcircuit Yields

2.5.1.1 Standard High-Performance Microcircuit Process

During this interim, refinements were made in our standard small-geometry, high-performance microcircuit fabrication process which have virtually eliminated the incidence of transistor emitter-base shorts. Yield analyses that were made on several lots of SMX14 wafers and on the first lot of ROM's have substantiated that transistor yield loss due to emitter-base diode degradation is consistently less than 1%. However, these same analyses revealed a transistor loss of 1% to 4% due to emitter-to-collector shorts. We believe these emitter-to-collector defects are due to n-type pipes which, due to process-induced material defects, locally penetrate the base during the emitter diffusion. Efforts are under way to minimize this cause of yield loss.

2.5.1.2 Collector Diffused Isolation (CDI) Process

It is well known that microcircuit yield is inversely related to microcircuit area and to the complexity of the fabrication

process. In principle, a reduction either in microcircuit area or in process complexity should give improved yield. In this interim we began an investigation to determine whether high-performance ECL microcircuits can be made at higher yield through use of simpler processing sequences. The specific process chosen is a form of the Collector Diffused Isolation (CDI) Process introduced by B. Murphy (see footnote on page 2). The chosen vehicle is a high-performance ECL gate. Figure 3 is the schematic diagram of this gate. Adaptation of this process to high-speed ECL has resulted in a 40% reduction in gate size and a substantial reduction in processing steps. (Only 5 photoengraving steps are required for the CDI Process as compared with 7 photoengraving steps for the standard process.)

The first group of CDI gates was completed late in this interim. Functional die sort indicated that gate yield was 50% overall, and 75% in the central high-yield portion of the wafer. A preliminary failure analysis indicated that yield loss in the "bad areas" was principally due to low transistor punch-through voltage. The low transistor punch-through voltage was due to nonuniformities in transistor base widths which, in turn, was a result of variations in the 1-μ epitaxial layer.

Epitaxial growth is extremely critical in the CDI Process for fabricating high-speed microcircuits, because any variation in

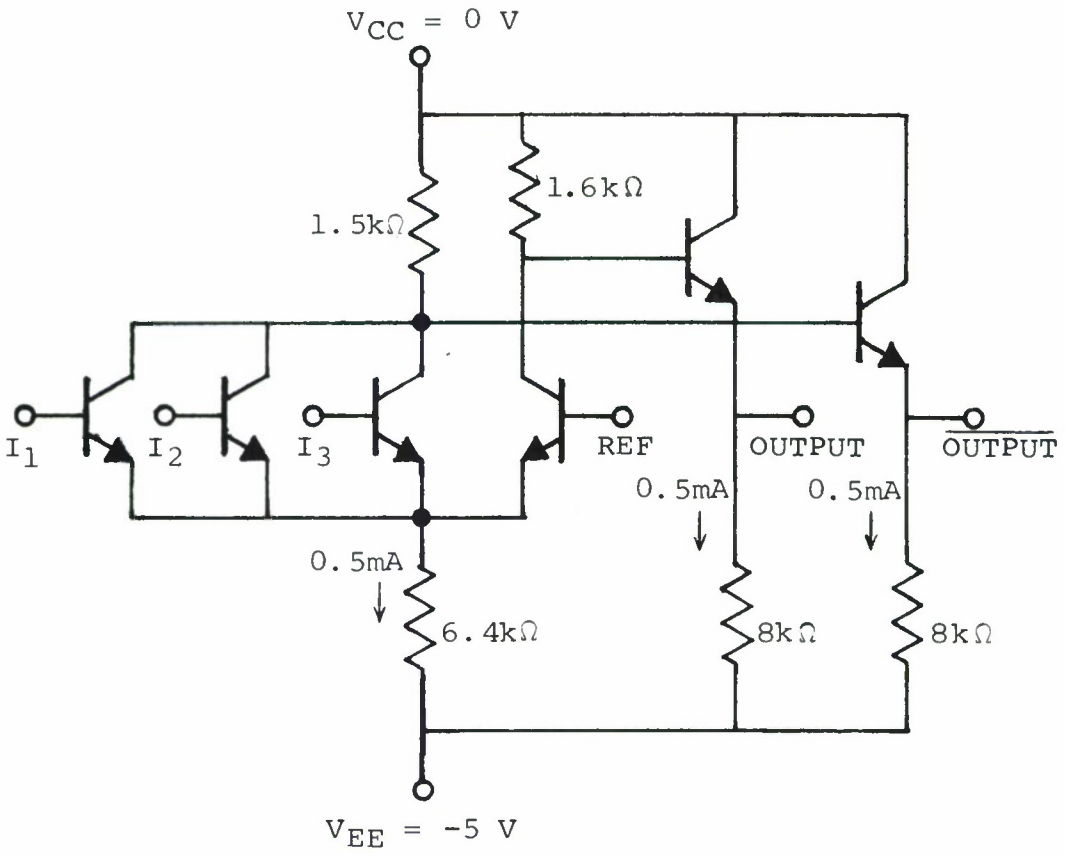

Figure 3. Circuit schematic for CDI-ECL gate.

epitaxial layer thickness across the wafer results in an identical variation in transistor base width. Since transistor base width is required to be less than 0.15 μ for high performance, it can be seen that fine control over the epitaxial growth process is essential to realizing the potential high-yield of this process. More detailed analyses are being performed and the results will be given in the next report. The analyses will include evaluation of the speed performance of the gates and their constituent transistors. Total power dissipation for these gates is about 7.5 mW. Performance of these gates will be compared with conventionally-processed high-speed ECL gates (SMX14 chips) which were sent to Lincoln Laboratory and which also have a nominal power dissipation of 7.5 mW. The transistor geometries are the same in both structures.

2.5.2 Multilevel Process Yields

The yield evaluations which were performed on SMX14 wafers included a characterization of the via test patterns. It was found that the present two-level design rules and two-level process were effective in producing low resistance vias between the first and second levels of metal. No via problems were encountered on any wafers of the three lots of wafers which were evaluated. Typical resistance per via (0.12 mil^2) was 67 mΩ.

Our present process and design rules for a three-level, small-geometry metallization system will be completely evaluated during

the next interim. The evaluation will be made on three-level arrays and on a Multilevel Process Test Chip, final design for the latter having been completed during this interim. Multilevel Process Test Chips are now being fabricated. This chip design will be used to examine via conductance and insulator integrity for a variety of via sizes and for a variety of substrate topographies for two- and three-level metal structures.

2.6 MULTICHIP ASSEMBLY TECHNIQUES

Photomask designs have been completed, and photomasks have been generated which adapt the Thermal Chip for evaluation of multichip assembly concepts such as face-down bonding and beam lead assembly. Structures representative of both concepts are being fabricated and are expected to be completed during the next interim. The Thermal Chip is particularly useful for this study because it permits accurate characterization of the thermal characteristics inherent in each of these assembly concepts; and further, because it has a pad density similar to that in the Processor Arrays.

2.7 ARRAY RELIABILITY DATA

Additional reliability data have been accumulated for two-level high-speed arrays (3-Bit Parity Arrays fabricated during the previous program). To date, 20 arrays have survived the following

sequences without any failures:

1. Temperature cycling, -55°C to 125°C, 25 cycles (each cycle consisted of 15 minutes at -55°C, 5 minutes at room temperature, and 15 minutes at 125°C);
2. Reverse bias life, 1000 hours at 125°C;
3. Functional life, 1000 hours at 125°C.

These arrays will be subjected to additional functional life testing during the next interim.

III - FUTURE WORK

Future work on this program will include:

1. Continued development of high-yield fabrication technologies for high-speed arrays. This effort will include detailed evaluation of multilevel processing using the Multilevel Chip.
2. Continued efforts to obtain an optimum-performance (in terms of speed and power) gate cell for the Processor Arrays.
3. Continued experiments to improve microcircuit yields. These experiments will be particularly aimed at reducing emitter-to-collector shorts in shallow-diffused transistors.
4. Fabrication and evaluation of additional Read-Only Memory Arrays.
5. Continued evaluation of the CDI Process for complex high-speed ECL array applications.
6. Fabrication of the Processor Master Array Chip.
7. Fabrication of the Loading Chip.
8. Continued investigation of face-down bonding and beam lead approaches to multichip assembly.
9. Continued thermal studies of high-power LSI Chips.

IV - DELIVERIES

The following were delivered to MIT Lincoln Laboratory during this interim:

1. Six packaged SMX14 test chips (each chip with gate dissipations of 15 mW and 7.5 mW),
2. Two packaged and programmed ROM's,
3. One wafer of ROM's,
4. Six packaged CDI gates,
5. Twelve packaged CDI test transistors.

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14. KEY WORDS
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Functioning Read-Only Memory Arrays
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CDI process for high speed ECL
Speed-power studies
aluminum beam leads
face-down bonding
reliability data